REMARKS

Claims 1-20 and 21-22 are pending in the application. By this Amendment, claims 1 and 6 are amended and claims 21 and 22 are added. Reconsideration and allowance in view of the following remarks are respectfully requested. Claims 1 and 6 are amended to address minor deficiencies. No new matter is added by this Amendment.

I. THE CLAIMS DEFINE PATENTABLE SUBJECT MATTER

The Office Action maintains the grounds of rejection set forth in the prior Office Action. Further, on page 3, the Office Action partially responds to Applicant's arguments as set forth in the July 14, 2003 Request for Reconsideration. This disposition set forth in the Office Action is respectfully traversed.

That is, for the reasons set forth below, Applicant traverses the comments of the Office Action in the "Response to Arguments" and traverses the maintained grounds of rejection.

A. Comments on the "Response to Arguments"

a. D'Arre

It is respectfully submitted that the applied art fails to teach or suggest the claimed invention. Rather, the Office Action is picking and choosing from distinct teachings of the applied art so as to allegedly teach the features of the claimed invention and the interrelationship set out in claim 1, for example. In particular, the applied art fails to teach or suggest the interrelationship between the sequential gating and the use of a current transformer, as claimed

On page 2, the Office Action asserts that Applicant's arguments filed 14 July 2003 have been fully considered but they are not persuasive. With regard to D'Arre, the Office Action

asserts that because in the remark page 5, Applicant argue about D'Aire does disclose the sequential gating and the use of a current transformer. In response, Applicant notes that on page 5, the July 14, 2003 Request for Reconsideration does reflect that D'Aire teaches the use of current transformers (page 5, line 20). However, the Office Action's reliance on Applicant's arguments is misplaced in that it is not seen where on page 5 Applicant discloses the claimed "sequential gating." The Examiner is requested to clarify the basis of such assertion and the language on page 4 (of the July 14, 2003 Request for Reconsideration) that is being used to support such assertion. In short, what is the Office Action interpreting to be the referenced sequential gating?

The Office Action further asserts that "[h]owever Applicant also indicated on page 4 of remark that column 6, line 27-35, discloses the circuit failure and abnormal operating condition fault detected by hardware implemented in the sensor assemblies; and the Office Action further asserts: "which also include the current transformer." The Office Action is respectfully requested to clarify where in the sensor assemblies 46 and 48, i.e., Figs. 2 and 3 of D'Aire, is the transformer (in that the presence of transformers in the sensor assemblies 46 and 48 is not apparent). Based on these deficiencies in the assertions in the Office Action, D'Aire fails to teach or suggest the claimed invention.

However, going beyond the misplaced assertions in the Office Action regarding D'Aire, Applicant notes that D'Aire teaches the use of current transformers, e.g., see column 6, lines 28 - 35 and as acknowledged in the July 14, 2003 Request for Reconsideration (page 5, line 19 - page

6, line 2). However, such disclosure of course falls short of teaching or suggesting the claimed invention and the specifics thereof, as recited in claim 1.

Claim 1 does not simply recite the use of current transformers to detect a shorted thyristor cell. Rather, claim 1 recites a particular approach to detecting a shorted thyristor cell including sequential gating. In the July 14, 2003 Request for Reconsideration, Applicant requested the Examiner clarify the basis of the rejection under 35 U.S.C. §102 based on D'Atre or withdraw the rejection. However, in response, it appears that the Office Action has fallen short of providing any sustainable position that D'Atre teaches the claimed invention. Rather, the Office Action appears to mischaracterize D'Atre and/or use Applicant's prior assertions so as to allegedly support the grounds of rejection.

b. Casteel

Further, the Office Action provides comments in the "Response to Arguments" regarding Casteel. That is, the Office Action reflects that "further in remark page 8, Applicant argue that Casteel does not disclose the utilization of sequentially gating of each cell, Examiner disagree column 1, line 45-55 of Casteel clearly indicating sequentially switching of switching device.

Applicant traverses these misplaced assertions. Applicant respectfully queries where on page 8 of the July 14, 2003 Request for Reconsideration does Applicant assert that Casteel "does not disclose the utilization of sequentially gating of each cell." Applicant acknowledges that Casteel, on page 1, line 46, for example, discusses sequential switching. However, similar to the above comments, the claimed invention as recited in claim 1 is not simply the general concept of

sequentially gating. Rather, claim 1 sets forth various features to effect the determination of a shorted thyristor cell, one of which is sequential gating.

The Office Action appears to be taking the position in the "Response to Arguments" that the claimed invention is taught under 35 U.S.C. §102 by either a teaching of a transformer for detecting cell failure faults (D'Aure) or a teaching of sequential gating. Such is of course not the test, in the art must teach each and every feature of the claimed invention - which it does not, as is further reinforced by the present Office Action. For these reasons, withdrawal of the rejection based on Casteel is respectfully requested.

c. Jadric

Further, the Office Action provides comments in the "Response to Arguments" regarding Jadric. The Office Action asserts that in Jadric et al.'s reference (column 1, line 5-65) similar method of sequentially trigger thyristors. Applicant submits that even if this were true, such teaching would of course fail to teach each and every feature of claim 1, i.e., in that claim 1 includes sequential gating, in conjunction with other features.

However, Applicant has reviewed column 1, line 5-65 of Jadric and simply cannot discern the teaching asserted in the Office Action. That is, where in column 1, line 5-65, does Jadric teach a method of sequentially trigger thyristors? For these reasons, withdrawal of the rejection based on Jadric is respectfully requested.

d. Fabianowski

In the July 14, 2003 Request for Reconsideration, Applicant set forth various grounds traversing the rejection under the teachings of Fabianowski. Further, Applicant notes that the

rejection under Fabianowski has been maintained in the present Office Action. However, the present Office Action appears fully devoid of addressing Applicant's remarks in any manner. Rather, the present Office Action merely repeats the Fabianowski based rejection, as set forth in the prior Office Action. Applicant respectfully requests that the Examiner address such grounds of traversal, as set forth in the July 14, 2003 Request for Reconsideration.

e. The Rejection under 35 U.S.C. §103

Further, the Office Action maintains the rejection of claims under 35 U.S.C. §103 based on Jadric in view of Casteel. However, the Office Action fails to address Applicant's traversal of those grounds of rejection, as such traversal is set forth in the July 14, 2003 Request for Reconsideration. It is respectfully submitted that the Office Action is quite simply not acknowledging Applicant's grounds of traversal, while maintaining the rejection.

f. The features of claim 6

In the July 14, 2003 Request for Reconsideration, Applicant noted that claim 6 recites the method of claim 4, further including the step of rectifying and scaling a current flow of the at least one current transformer that passes through the bridge, so that a signal level of the current flow that passes through the bridge is substantially that same as that of the shunt current signal value under non-shorted cell conditions. Applicant asserted that Fabianowski does not even appear to discuss a shunt. Accordingly, it is unclear how Fabianowski can teach the particular features of claim 6 under 35 U.S.C. §102. In a similar manner, it appears that D'Aire does not teach use of a shunt and thus fails to teach claim 6.

In the July 14, 2003 Request for Reconsideration, Applicant requested the Examiner to clarify where in the applied art are teachings of claim 6. However, the Office Action also appears devoid of any response to this query. Rather, the Office Action has simply repeated the grounds of rejection set forth in the prior Office Action.

f. The Added Claims 21 and 22

Claims 21 and 22 have been added to recite further novel features of the claimed invention. In particular such claims are directed to features wherein current transformer detection of a shorted thyristor cell is used in conjunction with shunt detection of a shorted thyristor cell.

B. Applicant Traverses the Grounds of Rejection Maintained in the Office Action

The grounds of rejection set forth in the Office Action corresponds to the grounds of rejection set forth in the prior February 12, 2003 Office Action. Applicant traverses such grounds of rejection for the reasons set forth above. That is, as discussed above, the Office Action sets forth no supportable basis to maintain the present grounds of rejection with respect to claim 1, and similarly with respect to the other independent claims. Accordingly, the remarks set forth in the July 14, 2003 Request for Reconsideration have been maintained below.

a. The Applied Art to Fabianowski or D'Atre

In the Office Action, claims 1-14 are rejected under 35 U.S.C. 102(b) as being anticipated by U.S. Patent # 4,942,494 to Fabianowski et al. (Fabianowski) or U.S. Patent # 4,475,150 to D'Atre et al. (D'Atre). This rejection is respectfully traversed.

Claim 1 recites a method for determining a shorted thyristor cell in a bridge that supplies a load from a source, the bridge including a plurality of the thyristor cells, the method including: sequentially gating each of the cells to a conducting state, so that only one cell is gated at one time; providing at least one current transformer in the bridge; generating a current flow that passes through the bridge including the one cell that is gated; observing current in the at least one current transformer to determine a short in one of the cells that is not gated; and determining a shorted cell based on the step of observing current in the at least one current transformer.

The Office Action sets out the claimed features of claim 1 and asserts that Fabianowski teaches such claimed features. The Office Action refers to the Abstract of Fabianowski.

In the Abstract, Fabianowski teaches that in a half-controlled three-phase bridge for feeding an inductive load, a further, externally charged capacitor and a further thyristor are additionally connected to the conventional protective capacitor which is already in existence. The further capacitor, which is charged from an external high-impedance voltage source, has the effect of causing an increased load current to be taken over by the further thyristor so that one of the conducting thyristors of the bridge is extinguished. The capacitor recharges and its voltage is used as a blocking voltage for the thyristor of the bridge which has just been extinguished so that the energy supply from the power system is stopped. Fabianowski teaches that the current in the load circuit can then be removed through a free-wheeling diode.

In contrast to the teachings of Fabianowski, claim 1 in particular recites sequentially gating each of the cells to a conducting state, so that only one cell is gated at one time; observing current in the at least one current transformer to determine a short in one of the cells that is not

gated; and determining a shorted cell based on the step of observing current in the at least one current transformer. These are very specific features directed to the novel aspects of the present invention. Fabianowski appears lacking of the claimed feature of the sequential gating. Further, Fabianowski appears lacking of the claimed feature of observing current in the at least one current transformer to determine a short in one of the cells that is not gated; and determining a shorted cell based on the step of observing current in the at least one current transformer. Accordingly, it is fully unclear how the Office Action's assertion, that the Fabianowski Abstract teaches the claimed invention, is supportable as a viable rejection.

Also, the other portions of Fabianowski have been reviewed and fail to teach or suggest the claimed invention. For example, Fabianowski in column 3, lines 49-65, teaches that when a short-circuit occurs in the load circuit 1, the short-circuit is detected by the control unit 3 through the current sensing devices 4, 5, 6. Fabianowski further describes that when an overcurrent is detected, the control unit 3 fires the thyristor T4 and thus switches the higher potential of the externally charged capacitor C to the load circuit. The firing pulses of the thyristors T1, T2, T3 are blocked simultaneously with the ignition of the thyristor T4 by the control mechanism 3. As a result, the current commutates from one of the conducting thyristors T1, T2 or T3 to the thyristor T4, that is to say the thyristor T4 takes over the increased load current which is currently flowing. However, this disclosure of Fabianowski also falls short of teaching or suggesting the specifics of claim 1.

Further, the Office Action asserts that D'Atre discloses the claimed subject matter. Applicant has reviewed the teachings of D'Atre. D'Atre is directed to a coordinated load

commuted inverter protection system. In column 5, lines 50-60, D'Atre teaches that, as shown in Fig. 1, a sensor assembly 46 has applied thereto the three source side phase to neutral voltages which are applied from voltage sensors 50, 51 and 52 coupled to the phase lines A_s, B_s and C_s while the three source side phase currents are generated by current sensors 54, 55 and 56. In addition to the three source side phase voltages and currents, the positive and negative voltages on the source side of the inductor 26 are coupled to the sensor assembly 46 by way of the voltage sensors 58 and 59.

In column 6, lines 27-35, D'Atre teaches that with respect to cell failure faults, the method of detecting the cell conduction pattern is by means of the appropriate microcomputer software in conjunction with thyristor cell state sensors and AC current transformers. Other circuit failures and abnormal operating condition faults are detected by the hardware implemented in the sensor assemblies 46 and 48 shown in Fig. 1. In column 6, D'Atre further teaches that as shown in Fig. 2 of D'Atre, all the comparator circuits 98, 100 . . . 110 have their other input commonly connected to a reference signal (REF). Depending upon the condition of each of the thyristor cells, the comparator circuits 98, 100 . . . 110 will output signals corresponding to either an ON or OFF state of the respective thyristor cell which is adapted to set or fail to set one of six flip-flops 112, 114, 116, 118, 120 and 122. D'Atre explains that these flip-flops accordingly generate high "one" or low "zero" digital signals corresponding to the thyristor ON/OFF state of each thyristor of the bridge.

D'Atre teaches further aspects of the D'Atre invention in column 20, line 50 - column 21, line 8. D'Atre teaches that because the source voltage is relatively fixed and the load voltage can

be relatively low at low motor speed, the LOAD SIDE PROTECT FIRE program is more complicated for the load side converter than the source side converter because in the load side converter, if the cell sensors indicate a conduction pattern fault, a double check is made by the load side current transformers to confirm the fault. D'Atre further explains that inasmuch as the aforementioned programs occur just before the firing of a new cell and because the firing angle of any cell can vary over a 180 degree range, the aforementioned "fire" programs are interrelated with two other programs which are substantially identical to one another in both microcomputers 34 and 36 and which occur at a fixed time relationship relative to the respective terminal or line to line voltages and more particularly the integral of the line to line voltages which on the load side of the system are referred to as pseudo flux waves.

However, Applicant has reviewed the teachings of D'Atre and submits that D'Atre fails to teach or suggest the features of claim 1. In particular, D'Atre fails to teach or suggest the interrelationship between the sequential gating and the use of a current transformer, as claimed.

Specifically, claim 1 recites a method for determining a shorted thyristor cell in a bridge including, for example, sequentially gating each of the cells to a conducting state, so that only one cell is gated at one time; observing current in the at least one current transformer to determine a short in one of the cells that is not gated; and determining a shorted cell based on the step of observing current in the at least one current transformer.

Based on Applicant's review of D'Atre it is fully unclear how the Office Action asserts that D'Atre teaches such claimed features. D'Atre does indeed teach the use of current transformers. However, such disclosure of course falls short of teaching or suggesting the

claimed invention and the specifics thereof. The Examiner is requested to clarify the basis of the rejection under 35 U.S.C. §102 based on D'Aire or withdraw the rejection.

Based on the above reasons, it is respectfully submitted that the applied art, either alone or in combination, fails to teach or suggest the features as set forth in claim 1.

Further, dependent claims 2-14 define patentable subject matter based on their various dependencies on claim 1, as well as the additional features such dependent claims recite. It is submitted that the applied art fails to teach or suggest the features of the dependent claims.

For example, claim 6 recites the method of claim 4, further including the step of rectifying and scaling a current flow of the at least one current transformer that passes through the bridge, so that a signal level of the current flow that passes through the bridge is substantially that same as that of the shunt current signal value under non-shorted cell conditions. Fabianowski does not even appear to discuss a shunt. Accordingly, it is unclear how Fabianowski can teach the particular features of claim 6 under 35 U.S.C. §102. In a similar manner, it appears that D'Aire does not teach use of a shunt and thus fails to teach claim 6. The Examiner is requested to clarify where in the applied art are teachings of claim 6.

Accordingly, it is respectfully submitted that the claims define patentable subject matter. Withdrawal of the rejection under 35 U.S.C. §102 is respectfully requested.

b. The Applied Art to Casteel or Jadric

In the Office Action, claims 1 and 15 are rejected under 35 U.S.C. 102(b) as being anticipated by U. S. Patent # 4,633,241 to Casteel et al. (Casteel) or U.S. Patent # 6,211,792 to

Jadric et al. (Jadric '792). The rejection based on the two references in the alternative is respectfully traversed.

The Office Action asserts that Casteel discloses all the claimed subject matters (column 1, line 40-70+); and that similarly Jadric's figure 1, discloses claimed subject matters (column 3, line 35-70).

With reference to Casteel, in column 1, lines 40-69, Casteel teaches a method of detecting shorted controllable switching devices in a bridge rectifier supplying a load and being supplied by AC power. Casteel describes that the method comprises the steps of first detecting the zero crossings of a voltage of the AC supply, and sequentially switching each of the controllable switching devices to the conductive state before the zero crossing of the voltage associated with the forward conduction of the controllable switching device, so that only one switching device is switched at a time. Next, the DC output voltage of the rectifier is measured after each of the controllable switching devices is switched to the conductive state. An indication of a shorted controllable switching device is provided when the DC output *voltage* is measured after each of the controlled switching devices is switched to the conductive state. Casteel further teaches a method comprising the steps of detecting the zero crossings of a voltage of the AC power and sequentially commanding pairs of controllable switching devices to switch to a conductive state, with each pair of controllable switching devices corresponding to a pair of switching devices conducting at the same time when a rectifier is operating in a line commutated mode.

However, it is respectfully submitted that Casteel does not teach the specifics of claim 1 with such disclosure. In particular, claim 1 recites sequentially gating each of the cells to a conducting state, so that only one cell is gated at one time; observing current in the at least one current transformer to determine a short in one of the cells that is not gated; and determining a shorted cell based on the step of observing current in the at least one current transformer. Such disclosure of Casteel simply does not teach such specifics and the interrelationship there between as is set forth in claim 1.

Applicant also notes column 3 of Casteel. Therein, Casteel teaches that an analog zero crossing detector circuit 20 is coupled by high resistance isolation to 2 of the 3 phase AC lines and provides an interrupt signal to a microprocessor 21 when a zero crossing of the phase to phase voltage is detected. Microprocessor 21 can comprise a plurality of Intel 8031 microcomputers. Casteel further describes that an armature voltage isolator 23 is coupled across the output of the dual rectifier bridge 13 and provides a filtered analog signal to an analog multiplexer 25. An armature current isolator is coupled across shunt 19.

Casteel further describes that, alternatively, current can be measured by using current transformers in two of the three AC lines; and that armature current isolator 27 provides an analog signal proportional to armature current to analog multiplexer 25. In further explanation of such features of the Casteel invention, Casteel teaches, in column 3, lines 38-43, that Microprocessor 21 provides gate pulse signals to gate pulse amplifier 41 which in turn are coupled to the gates of the 12 SCRs in dual bridges 13; and that a firing timer 43, which is part of

microprocessor 21 provides an interrupt when the counter overflows, indicative of the next SCR firing time.

However, it is submitted that such features simply do not teach the invention as recited in claim 1. In particular, such disclosure of Casteel does not teach sequentially gating each of the cells to a conducting state so that only one cell is gated at one time; observing current in the at least one current transformer to determine a short in one of the cells that is not gated; and determining a shorted cell based on the step of observing current in the at least one current transformer. The Examiner is respectfully requested to clarify where in Casteel such particulars are set forth.

Further, Applicant notes that Casteel describes a test process in column 4, lines 32-69. For example, Casteel teaches that assuming the test starts with SCR 3F as shown in FIG. 5, SCR 3F will be gated with a single pulse. At ten degrees after the firing, the armature current, or alternatively line currents if current transformers are connected to two of the three AC lines, and voltage are sampled with the armature voltage being used in the short circuit test as hereinafter described. Casteel teaches that the analog speed reference and feedback from the tachometer are read, but not used during the short circuit test. At 21, 30 and 43 degrees after firing, the armature current in the shunt is sampled but not used in the short circuit test. The voltage measured at ten degrees after firing which is close to the phase to phase voltage zero crossing is compared to a threshold value to see of any *voltage* appears across the motor which would indicate a shorted SCR. Accordingly, Casteel teaches observing voltage across the motor.

Casteel further explains that there are two possibilities of current being generated as a result of one cell being shorted somewhere in the dual bridge besides the SCR that has just been gated. Current could flow directly from the gated SCR to the shorted SCR on the same side of the motor and out to the power supply, in which case a short circuit would be detected when the appropriate SCR on the opposite side of the motor is fired, or it could flow from the gated SCR through the motor through the shorted SCR and out to the 3 phase power source. Casteel describes that in the second situation the voltage across the motor would be detected. For example, consider a possible current path when SCR 1F is gated on during phase to phase voltage AC. If SCR 3F or 6R were shorted, the current would flow directly from phase A, through SCR 1F through the motor, and then through 6F or 3R and out into phase C.

In particular, Casteel teaches that the shorted cell is detected by measuring the filtered *voltage* across the motor at or near the phase to phase voltage zero crossing after cross firing. Any voltage measured above a small threshold to allow for electrical noise indicates a short. When a fault is detected, a look up table based on the cell fired is used to determine the correct fault code which is saved. The short circuit test is repeated to reinforce the findings of the first test when a fault is detected. The test is repeated by restarting the test with the next cell and continuing until twelve cells have been gated.

It is respectfully submitted that claim 1 recites very specific features relating to the sequential gating and determining a shorted cell based on the step of observing current in the at least one current transformer. The Office Action simply asserts that Casteel discloses all the claimed subject matter. However, as discussed above, Applicant has reviewed the teachings of

Casteel that were identified by the Office Action, as well as the other portions of Casteel. It is respectfully submitted that Casteel does not suggest or render obvious the claimed invention. Moreover, it is submitted that Casteel in no way teaches the claimed features so as to support a rejection of claim 1 under 35 U.S.C. §102(b). Withdrawal of the rejection based on Casteel is respectfully requested.

The Office Action also rejects claim 1 based on the teachings of Jadric 792. The Office Action asserts that Jadric 792's Fig. 1, discloses the claimed subject matters (column 3, line 35-70).

In column 2, lines 54-64, Jadric 792 teaches that Fig. 1 is a schematic diagram of a three phase alternating current power supply 112 for a load 102 with a reduced voltage solid state starter or controller 150. Load 102 may comprise a three phase motor, which may drive various components of a refrigeration system. Further, in column 3, lines 18-37, Jadric 792 teaches an arrangement wherein a first fault detector 110 is in parallel with first thyristor pair 104, a second fault detector 114 is in parallel with second thyristor pair 106, and a third fault detector 116 is in parallel with third thyristor pair 108. Each detector 110, 114, and 116 detects faults in thyristor pairs 104, 106, or 108, respectfully.

In column 3, Jadric 792 further teaches Fig. 3 is a more detailed circuit diagram of thyristor pair 104 in parallel with first fault detector 110 as shown in Fig. 1; and that a first fault detector 110 comprises a bidirectional photo-coupler 310 in series with a capacitor 320 and a resistor 314. Jadric further describes a bidirectional photo-coupler 310 comprises a light

emitting diode (LED) pair 316, 318 arranged in a back-to-back configuration, and an optically-sensitive bipolar junction transistor (BJT) 308.

Further, in column 4, Jadric describes further aspects of fault detection. That is, Jadric teaches a second fault detection circuit 114, and third fault detection circuit 116 operate similarly to first fault detection circuit 110. Jadric further teaches that a microprocessor 326 analyzes the logic pulses from fault detection circuits 110, 114, and 116 to detect if any of thyristors 142-147 has failed.

The Office Action asserts that Jadric 792 teaches the claimed subject matter. However, it is respectfully submitted that the teachings as set out above, as well as the other teachings of Jadric fail to teach or suggest the invention as recited in claim 1. In particular, claim 1 recites sequentially gating each of the cells to a conducting state, so that only one cell is gated at one time; observing current in the at least one current transformer to determine a short in one of the cells that is not gated; and determining a shorted cell based on the step of observing current in the at least one current transformer. Such disclosure of Jadric simply does not teach such specifics and the interrelationship there between.

As with Casteel discussed above, it is fully unclear how the Office Action asserts that Jadric teaches the features of claim 1. The Examiner is respectfully requested to clarify the manner in which each and every feature of claim 1 is disclosed in Jadric 792.

Based on the above reasons, it is respectfully submitted that the applied art, either alone or in combination, fails to teach or suggest the features as set forth in claim 1. Further, it is

respectfully submitted that claim 15 defines patentable subject matter for reasons similar to those set forth above with respect to claim 1.

Accordingly, it is respectfully submitted that the claims define patentable subject matter. Withdrawal of the rejection under 35 U.S.C. §102 is respectfully requested.

c. The Rejection of Claims 1-20 Over Jadric in Combination with Casteel

Claims 1-20 are rejected under 35 U.S.C. 103(a) as being unpatentable over U. S. Patent # 6,404,346 to Jadric (Jadric 346) in combination with Casteel.

The Office Action asserts that Jadric 346 discloses the claimed invention a method for determining a shorted thyristor cell in a bridge that supplies a load from a source, but that however Jadric detects a fail thyristor by utilizing method of measuring an instantaneous power delivered to the load during a cycle of the input. The Office Action further asserts that Jadric does not disclose utilization of a technique for a gate sequencing. The Office Action then asserts that Casteel teaches utilization of similar technique for a gate sequencing (column 1, line 40-70).

The Office Action further asserts that it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify Jadric's method of detecting failed thyristor by utilizing a technique taught by Casteel, for the purpose of providing an efficient, low voltage, high current switching regulator circuit that have low input and output ripple currents. These assertions as set forth in the Office Action are respectfully traversed.

The teachings of Casteel are described above. Further, the particular features of claim 1 are described above.

In the Abstract, Jadric 346 teaches that a method for detecting if a thyristor failed open in an alternating current input phase of a load comprises measuring an instantaneous power delivered to the load during a cycle of the input; determining a peak power delivered to the load during the cycle of the input; calculating an average power delivered to the load during the cycle of the input; and determining if the thyristor failed open by comparing the magnitudes of the peak power and the average power.

The Office Action acknowledges that Jadric 346 does not disclose utilization of a technique for gate sequencing.

In the "Background of the Invention," Jadric 346 teaches aspects of failure of a resistor. In particular, Jadric teaches that failure of a thyristor in the starter may also result in poor motor functioning. Thyristor failures generally result in unbalanced power supply conditions, which may lead to large torque oscillations that can damage mechanical couplings and gears driven by the motor. Jadric 346 further teaches that some present day thyristor failure detectors use an electronic circuit intended to detect an open thyristor fault, i.e., when the thyristor fails to conduct when it is intended. These thyristor failure detectors indirectly measure three currents through three supply lines by measuring three voltages generated by current transformers in the supply lines.

In column 4, lines 44-59, Jadric further teaches aspects of the thyristor pairs of the Jadric invention. Jadric teaches that if any thyristor 142-148 of thyristor pairs 104, 106, or 108 in any line 130, 132, or 136 fails open, i.e., fails to conduct, then the line with the failure carries only unidirectional current with an AC and a non-zero DC component. Further, if any thyristor 142-

148 fails open, all three of line currents Ia, Ib, and Ic have an AC and a non-zero DC component. Jadric 346 further describes that ammeters 114 and 116 cannot detect the DC components of the current in the steady state, but they can detect the DC component for 30 to 130 microseconds during the transition after the failure event. This transition time period is determined by the current transformer design and the value of the transformer resistor. Thus, Jadric teaches, that 30 to 130 microseconds after a failed open condition, ammeters 114 and 116 detect only the AC component of the current, whose value is almost unaffected by the fault.

Accordingly, Jadric teaches that such transition time period is determined by the current transformer design. Further, Jadric teaches that thyristor failure detectors indirectly measure three currents through three supply lines by measuring three voltages generated by current transformers in the supply lines. However, Applicant submits that Jadric fails to tech or suggest the claimed feature of "observing current in the at least one current transformer to determine a short in one of the cells that is not gated; and determining a shorted cell based on the step of observing current in the at least one current transformer." Further, Casteel fails to teach or suggest such features, as discussed above. Accordingly, even if the applied art were somehow combined, it is submitted that the combination would fail to teach the claimed invention.

Applicant submits that the sequential gating of the cells is an integral part of the claimed invention, as recited in the present claim 1. As noted in the Office Action Jadric fails to teach utilization of techniques for gate sequencing. The Office Action asserts that it would have been obvious to combine the teachings of the applied art so as to teach the claimed invention, i.e., as the Office Action asserts, by utilizing a technique as taught by Casteel. However, it is submitted

that there is simply no motivation or suggestion in the art so as to support the combination as asserted in the Office Action.

As noted above, Jadric teaches, for example, that thyristor failure detectors indirectly measure three currents through three supply lines by measuring three voltages generated by current transformers in the supply lines. There is simply no motivation to modify these teachings, nor the other teachings of Jadric 346 with the switching techniques of Casteel so as to teach or suggest the claimed invention.

Further, it is respectfully submitted that it is not even clear how the applied art would be combined as proposed in the Office Action. The Examiner is requested to clarify the manner in which the applied art would allegedly be combined, i.e., such as what features of Jadric 346 would Casteel replace.

Based on the above reasons, it is respectfully submitted that the applied art, either alone or in combination, fails to teach or suggest the features as set forth in claim 1. Further, it is respectfully submitted that claim 15 defines patentable subject matter for reasons similar to those set forth above with respect to claim 1.

Further, claim 15 teaches particulars of the claimed invention relating to a shunt. Casteel teaches that the analog speed reference and feedback from the tachometer are read but not used during the short circuit test; and at 21, 30 and 43 degrees after firing, the armature current in the shunt is sampled but not used in the short circuit test, for example, as described in column 4 of Casteel. However, Casteel fails to teach the particulars of the interrelationship of the shunt, as recited in claim 15. Moreover, Casteel fails to teach the further details of the shunt recited in

claim 19. Jadric 346 appears silent as to the use of a shunt, and thus cannot cure the deficiencies of Casteel.

Dependent claims 2-14 and 16-20 define patentable subject matter based on their various dependencies on the independent claims, as well as the additional features such dependent claims recite. It is submitted that the applied art fails to teach or suggest the features of the dependent claims.

Accordingly, it is respectfully submitted that the claims define patentable subject matter. Withdrawal of the rejection under 35 U.S.C. §103 is respectfully requested.

II. CONCLUSION

For at least the reasons outlined above, Applicant respectfully asserts that the application is in condition for allowance. Favorable reconsideration and allowance of the claims are respectfully solicited.

Should the Examiner believe anything further is desirable in order to place the application in even better condition for allowance, the Examiner is invited to contact Applicant's undersigned representative at the telephone number listed below.

For any further fees due in connection with filing this Response the Commissioner is hereby authorized to charge the undersigned's Deposit Account No. 50-0206.

Respectfully submitted,
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